REMARKS

Claims 1-22 are pending in the application. Figure 1 is objected to. The Specification is objected to. Claims 9, 12, 15, 18 and 22 are objected to. Claims 1-5, 9-11 and 14 are rejected under 35 U.S.C. §102(e). Claims 6-8, 12-13 and 15-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 20-22 are allowed. Applicants address these objections and rejections below.

Applicants amended claims 9, 12 and 15 to more clearly define the claimed subject matter and not to overcome prior art. Further, Applicants amended claim 20 to correct a typographical mistake. Hence, no prosecution history estoppel arises from the amendments to claims 9, 12, 15 and 20. *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 62 U.S.P.Q.2d 1705, 1711-12 (2002); 56 U.S.P.Q.2d 1865, 1870 (Fed. Cir. 2000). Further, the amendments made to claims 9, 12, 15 and 20 were not made for a substantial reason related to patentability and therefore no prosecution history estoppel arises from such amendments. *See Festo Corp.*, 62 U.S.P.Q.2d 1705 at 1707 (2002); *Warner-Jenkinson Co. v. Hilton Davis Chemical Co.*, 41 U.S.P.Q.2d 1865, 1873 (1997).

I. OBJECTIONS TO THE DRAWINGS:

The Examiner has objected to Figure 1 for lacking the legend of "Prior Art." Office Action (6/5/2006), page 2. Applicants amended Figure 1 to include the legend of "Prior Art." Accordingly, Applicants respectfully request the Examiner to withdraw the objection to Figure 1.

II. OBJECTIONS TO THE SPECIFICATION:

The Examiner has objected to the Specification for allegedly including confusing language and improper citations to Figure elements as indicated on page 2 of the Office Action. Office Action (6/5/2006), page 2. Applicants have appropriately amended the Specification to correct these deficiencies. Accordingly,

Applicants respectfully request the Examiner to withdraw the objections to the Specification.

III. OBJECTIONS TO THE CLAIMS:

The Examiner has objected to the language of "indicating layouts" in claim 9 for lack of clarity. Office Action (6/5/2006), page 2. Applicants have amended claim 9 to more clearly define the claimed subject matter.

The Examiner has further objected to claims 12 and 15 for lack of clarity as far as which step in claim 11 they further define. Office Action (6/5/2006), page 2. Applicants have amended claims 12 and 15 to more clearly define the claimed subject matter.

The Examiner has further objected to the limitation of "being indicative of layout patterns that fail at least one ORC demonstrating good and poor manufacturability" in claim 18 for allegedly lacking antecedent basis. Office Action (6/5/2006), page 2. Applicants respectfully assert that claim 18 does not lack antecedent basis. The phrase pointed out by the Examiner refers to the graphical representation which has been previously used in claim 18. Hence, there is no lack of antecedent basis in claim 18.

The Examiner has further objected to the limitation of "at least one pre-existing design rule from the current technology" in claim 22 as allegedly lacking antecedent basis. Office Action (6/5/2006), page 2. Applicants respectfully assert that claim 22 does not lack antecedent basis. "Current technology" is referred to in claim 20 and hence the phrase pointed out by the Examiner does not lack antecedent basis.

Consequently, Applicants respectfully request the Examiner to withdraw the objections to claims 9, 12, 15, 18 and 22.

IV. REJECTIONS UNDER 35 U.S.C. §102(e):

The Examiner has rejected claims 1-3, 5 and 9-10 under 35 U.S.C. §102(e) as being anticipated by Galan et al. (U.S. Patent No. 6,899,981) (hereinafter "Galan"). The Examiner has further rejected claims 1-5, 10-11 and 14 under 35 U.S.C. §102(e)

as being anticipated by Misaka et al. (U.S. Patent No. 6,691,297) (hereinafter "Misaka"). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

A. Claims 1-3, 5 and 9-10 are not properly rejected under 35 U.S.C. §102(e) as being anticipated by Galan.

Applicants respectfully assert that Galan does not disclose "generating an initial layout corresponding to the IC device design, said initial layout complying with a predetermined set of design rules" as recited in claim 1. The Examiner cites column 4, line 47 of Galan as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 3. Applicants respectfully traverse and assert that Galan instead discloses generating a mask pattern file. Column 4, line 47. There is no language in the cited passage that discloses that the mask pattern file complies with a predetermined set of design rules. Thus, Galan does not disclose all of the limitations of claim 1, and thus Galan does not anticipate claim 1. M.P.E.P. §2131.

Applicants further assert that Galan does not disclose "simulating how structures within the initial layout will pattern on a wafer" as recited in claim 1. The Examiner cites column 4, lines 47-59 of Galan as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 3. Applicants respectfully traverse and assert that Galan instead discloses that once the mask pattern file has been generated, a mask rule checking (MRC) system may be used to measure dimensions of various critical features in the mask pattern file. Column 4, lines 47-49. Galan further discloses that the MRC system may compare the measured dimensions to one or more manufacturing rules associated with a specific manufacturing process. Column 4, lines 49-52. Hence, Galan discloses that using a mask rule checking system to measure dimension of various critical features in the mask pattern file and comparing those measured dimensions to one or more manufacturing rules. There is no language

in the cited passage that discloses simulating structures. Neither is there any language in the cited passage that discloses simulating how structures within the initial layout will pattern on a wafer. Thus, Galan does not disclose all of the limitations of claim 1, and thus Galan does not anticipate claim 1. M.P.E.P. §2131.

Applicants further assert that Galan does not disclose "identifying portions of the simulated layout which demonstrate poor manufacturability" as recited in claim 1. The Examiner cites column 4, lines 50-59; column 6, lines 53-56; column 8, lines 39-41; and column 9, lines 8-12 of Galan as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 3. Applicants respectfully traverse.

Galan instead discloses that the MRC system may compare the measured dimensions to one or more manufacturing rules associated with a specific manufacturing process. Column 4, lines 49-52. Galan further discloses that the MRC system compares the measured dimensions with the calculated rules to determine if the manufacturing processes may be used to fabricate a photomask from the mask pattern file. Column 6, lines 53-56. Galan additionally discloses that the measured dimensions from the mask pattern file are compared to the respective manufacturing rules for the possible manufacturing processes. Column 8, lines 39-41. Furthermore, Galan discloses that these measured values are then compared to the manufacturing rules for the various manufacturing processes to determine which manufacturing processes may be acceptable to manufacture photomask 12 with the specific mask pattern file. Column 9, lines 8-12. Hence, Galan discloses that using a mask rule checking system to measure dimension of various critical features in the mask pattern file and comparing those measured dimensions to one or more manufacturing rules. There is no language in the cited passages that discloses identifying portions of a simulated layout. Neither is there any language in the cited passages that discloses identifying portions of the simulated layout which demonstrate poor manufacturability. Thus, Galan does not disclose all of the limitations of claim 1, and thus Galan does not anticipate claim 1. M.P.E.P. §2131.

Applicants further assert that Galan does not disclose "creating at least one design rule to disallow at least one portion of the layout identified in step (c)" as recited in claim 1. The Examiner cites column 5, lines 1-3, 15-18; column 6, lines 1-3, 25-30, 50-53, 59-64; column 7, lines 27-31; and column 9, lines 8-21 of Galan as disclosing the above-cited claim limitation. Office Action (6/5/206), page 3. Applicants respectfully traverse.

Galan instead discloses that the manufacturing rules may be calculated based on a design parameter associated with the selected manufacturing process. Column 5, lines 1-3. Galan further discloses that if the MRC system determines that the mask pattern file includes feature dimensions that are less than the manufacturing rules for the selected manufacturing process, rule violations may be identified in the mask pattern file. Column 5, lines 15-18. Galan additionally discloses that if the measured dimensions are less than the manufacturing rules for any given manufacturing process, rule violations may be identified in the mask pattern file and the mask pattern file may not be used to create photomask 12 with the corresponding manufacturing process. Column 6, lines 25-30. Galan further discloses a MRC system measures dimensions of critical features in a mask pattern file and calculates manufacturing rules for each possible manufacturing process that may be used to form features from the mask pattern file on a photomask. Column 6, lines 49-53. Furthermore, Galan discloses that the MRC system calculates manufacturing rules for each possible manufacturing process that may be used to fabricate a photomask from the mask pattern file. Column 7, lines 27-29. Additionally, Galan discloses that these measured values are then compared to the manufacturing rules for the various manufacturing processes to determine which manufacturing processes may be acceptable to manufacture photomask 12 with the specific mask pattern file. Column 9, lines 8-12. Hence, Galan discloses that if the mask pattern file includes feature dimensions that are less than the manufacturing rules for the selected manufacturing process, rule violations may be identified in the mask pattern file.

There is no language in the cited passages that discloses creating at least one design rule. Neither is there any language in the cited passages that discloses creating

at least one design rule to disallow at least one portion of the layout identified in step (c). Thus, Galan does not disclose all of the limitations of claim 1, and thus Galan does not anticipate claim 1. M.P.E.P. §2131.

Claims 2-3, 5 and 9-10 each recite combinations of features of independent claim 1, and thus claims 2-3, 5 and 9-10 are not anticipated by Galan for at least the reasons that claim 1 is not anticipated by Galan.

Applicants further assert that Galan does not disclose "producing a layout complying with the design rules created at step (d)" as recited in claim 2. The Examiner cites column 5, lines 30-43; column 6, lines 56-59; and column 9, lines 25-30 of Galan as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 3. Applicants respectfully traverse and assert that Galan instead discloses that once the mask pattern file has been checked to verify that it may be used with the selected manufacturing process, the desired pattern may be imaged into a resist layer of the photomask blank using a laser, electron beam or X-ray lithography system. Column 5, lines 30-34. Galan further discloses that if the measured dimensions are greater than or equal to the calculated manufacturing rules for at least one of the manufacturing processes, the mask pattern file may be used to fabricate the photomask. Column 6, lines 56-59. Galan additionally discloses that the identified violations may be fixed in the mask pattern file by notifying the integrated circuit designer that generated the mask layout file and having the designer make any necessary changes. Column 9, lines 26-29. Hence, Galan discloses that once the mask pattern file has been checked to verify that it may be used with the selected manufacturing process, the desired pattern may be imaged into a resist layer of the photomask blank. There is no language in the cited passages that discloses producing a layout complying with the design rules created at step (d). Thus, Galan does not disclose all of the limitations of claim 2, and thus Galan does not anticipate claim 2. M.P.E.P. §2131.

Applicants further assert that Galan does not disclose "simulating how structures within the layout produced at step (e) will pattern on a wafer" as recited in

claim 2. The Examiner cites column 4, lines 47-59 and column 6, lines 59-64 of Galan as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 3. Applicants respectfully traverse and assert that Galan instead discloses that once the mask pattern file has been generated, a mask rule checking (MRC) system may be used to measure dimensions of various critical features in the mask pattern file. Column 4, lines 47-49. Galan further discloses that if the measured dimensions are less than all of the calculated manufacturing rules, the mask pattern file may be removed from the manufacturing process until rule violations associated with at least one of the manufacturing rules are eliminated. Column 6, lines 59-64. There is no language in the cited passages that discloses simulating how structures within the layout produced at step (e) will pattern on a wafer. Thus, Galan does not disclose all of the limitations of claim 2, and thus Galan does not anticipate claim 2. M.P.E.P. §2131.

Applicants further assert that Galan does not disclose "repeating steps (c)-(f) until no portions of the simulated layout demonstrate poor manufacturability" as recited in claim 3. The Examiner cites Figure 3 of Galan as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 3. Applicants respectfully traverse. There is no language in the description of Figure 3 that discloses repeating steps (c)-(f). Neither is there any language in the description of Figure 3 that discloses repeating steps (c)-(f) until no portions of the simulated layout demonstrate poor manufacturability. Thus, Galan does not disclose all of the limitations of claim 3, and thus Galan does not anticipate claim 3. M.P.E.P. §2131.

Applicants further assert that Galan does not disclose "performing at least one optical proximity correction (OPC) on the layout before performing step (b)" as recited in claim 5. The Examiner cites column 3, lines 34-37 of Galan as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 3. Applicants respectfully traverse and assert that Galan instead discloses that the photomask 12 may further be a binary mask, a phase shift mask (PSM), an optical proximity correction (OPC) mask or any other type of mask suitable for use in a lithography system. Column 3, lines 34-37. While Galan discloses an optical proximity

correction (OPC) mask, there is no language in the cited passage that discloses performing at least one optical proximity correction (OPC) on the layout before performing step (b). Thus, Galan does not disclose all of the limitations of claim 5, and thus Galan does not anticipate claim 5. M.P.E.P. §2131.

Applicants further assert that Galan does not disclose "providing a graphical representation indicating portions of the simulated layout identified in step (c)" as recited in claim 9. The Examiner cites column 5, lines 20-21 and column 9, lines 22-25 of Galan as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 3. Applicants respectfully traverse and assert that Galan instead discloses that the violations may be graphically represented on a display screen associated with the MRC system. Column 5, lines 20-21. Galan further discloses that the features in the mask pattern file may be graphically displayed on a display screen and a rule violation may be indicated by a cross, circle, square or any other appropriate shape that may graphically represent the rule violation. Column 9, lines 22-25. Hence, Galan discloses graphically representing violations as well as graphically representing features in the mask pattern file. However, there is no language in the cited passages that discloses providing a graphical representation indicating portions of the simulated layout identified in step (c). Thus, Galan does not disclose all of the limitations of claim 9, and thus Galan does not anticipate claim 9. M.P.E.P. §2131.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within Galan, and thus claims 1-3, 5 and 9-10 are not anticipated by Galan. M.P.E.P. §2131.

B. Claims 1-5, 10-11 and 14 are not properly rejected under 35 U.S.C. §102(e) as being anticipated by Misaka.

Applicants respectfully assert that Misaka does not disclose "creating at least one design rule to disallow at least one portion of the layout identified in step (c)" as recited in claim 1 and similarly in claim 11. The Examiner cites column 13, line 58 – column 4, line 14, 43 of Misaka as disclosing identifying portions of the simulated layout which demonstrate poor manufacturability. Office Action (6/5/2006), page 4. The Examiner further cites column 15, lines 28-33 and column 16, lines 20-21, 27-28

of Misaka as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 4. Applicants respectfully traverse.

Misaka instead discloses in step SB7 (Please see Figure 2 of Misaka) it is determined whether or not each of the OPC patterns that have been made in Step SB6 shown in Figure 2 meets the OPC pattern placement rules set in step SB1. Column 13, lines 58-61. Misaka further discloses that if the OPC pattern placement rules are not met in this manner, then the method proceeds to step SB8 shown in Figure 2. Column 13, lines 65-67. Misaka further discloses that in step SB8, the OPC pattern specifications are modified such that the OPC pattern placement rules are also met in the region 17. Column 13, line 67 – column 14, line 2. Misaka additionally discloses that to eliminate the violation of the rule in the region 17 shown in Figure 4, the specifications should be modified by changing the shapes of the respective OPC patterns 12 through 14 depending on the distance between adjacent patterns. Column 14, lines 3-7. Hence, Misaka discloses that if the OPC pattern placement rules are not met (Examiner asserts that this is equivalent to identifying portions of the simulated layout which demonstrate poor manufacturability) then the OPC pattern specifications are modified. A design rule is not created to disallow at least one portion of the layout identified which demonstrated poor manufacturability. Thus, Misaka does not disclose all of the limitations of claims 1 and 11, and thus Misaka does not anticipate claims 1 and 11. M.P.E.P. §2131.

The Examiner's citation to column 15, lines 28-33 and column 16, lines 20-21, 27-28 of Misaka refers to step SB12 of Figure 2 which only occurs when the OPC pattern placement rules are met (See "yes" branch from step SB7 in Figure 2). Hence, step SB12 only occurs when there are no portions of the simulated layout demonstrate poor manufacturability (Examiner asserts that when the OPC pattern placement rules are not met that this is equivalent to identifying portions of the simulated layout which demonstrate poor manufacturability). Hence, Misaka does not disclose creating a design rule to disallow at least one portion of the layout identified which demonstrated poor manufacturability. Thus, Misaka does not disclose all of the limitations of claims 1 and 11, and thus Misaka does not anticipate claims 1 and 11. M.P.E.P. §2131.

Applicants further assert that Misaka does not disclose "generating a plurality of parametrically varying layout patterns" as recited in claim 11. The Examiner cites column 16, lines 36-44 of Misaka as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 4. Applicants respectfully traverse and assert that Misaka instead discloses that that multiple circuits (or cells) are prepared as typical samples to be registered at a cell library, thereby realizing a target circuit area of the cell library of the current generation. Column 16, lines 36-40. Hence, Misaka discloses preparing multiple circuits as samples of a target circuit area. In other words, Misaka discloses preparing samples of different sections of a target circuit area. This is not the same as generating a plurality of parametrically varying layout patterns. Thus, Misaka does not disclose all of the limitations of claim 11, and thus Misaka does not anticipate claim 11. M.P.E.P. §2131.

Applicants further assert that Misaka does not disclose "simulating how each layout pattern will pattern on a wafer" as recited in claim 11. The Examiner had previously cited column 16, lines 36-44 of Misaka as disclosing a parametrically varying layout patterns. Office Action (6/5/2006), page 4. The Examiner further cites column 13, lines 7-21 of Misaka as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 4. Applicants respectfully traverse.

Misaka instead discloses that in step SB5, specifications of OPC patterns to be made are set with respect to the circuit patterns. Column 13, lines 7-8. Misaka further discloses that the OPC pattern specifications may be set by any known technique, i.e., no matter whether the technique is rules-based or models-based. Column 13, lines 8-11. There is no language in the cited passage that discloses simulating how each sample to be registered at a cell library (Examiner asserts that these samples, as discussed in column 16, lines 36-39, are equivalent to varying layout patterns) will pattern on a wafer. Thus, Misaka does not disclose all of the limitations of claim 11, and thus Misaka does not anticipate claim 11. M.P.E.P. §2131.

Applicants further assert that Misaka does not disclose "classifying edges of structures within the simulated layout patterns based on manufacturability" as recited

in claim 11. The Examiner cites column 13, lines 15-16, 58 – column 4, line 14; and column 16, lines 54-57 of Misaka as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 4. Applicants respectfully traverse.

Misaka instead discloses that rules of making an OPC pattern are defined for each pattern category of the circuit pattern. Column 13, lines 15-16. Misaka further discloses that in step SB7 (Please see Figure 2 of Misaka) it is determined whether or not each of the OPC patterns that have been made in step SB6 shown in Figure 2 meets the OPC pattern placement rules set in step SB1. Column 13, lines 58-61. Misaka additionally discloses that if the OPC pattern placement rules are not met in this manner, then the method proceeds to step SB8 shown in Figure 2. Column 13, lines 65-67. In addition, Misaka discloses that in step SB8, the OPC pattern specifications are modified such that the OPC pattern placement rules are also met in the region 17. Column 13, line 67 – column 14, line 2. Misaka additionally discloses that to eliminate the violation of the rule in the region 17 shown in Figure 4, the specifications should be modified by changing the shapes of the respective OPC patterns 12 through 14 depending on the distance between adjacent patterns. Column 14, lines 3-7. Misaka further discloses that design rules are finally determined such that the conditions that should be met to make the OPC effective are also reflected on-design rules defined to design circuit patterns belonging to several typical categories. Column 16, lines 54-57. Hence, Misaka discloses that if the OPC pattern placement rules are not met then the OPC pattern specifications are modified. There is no language in the cited passages that discloses classifying edges of structures. Neither is there any language in the cited passages that discloses classifying edges of structures within the simulated layout patterns. Neither is there any language in the cited passages that discloses classifying edges of structures within the simulated layout patterns based on manufacturability. Thus, Misaka does not disclose all of the limitations of claim 11, and thus Misaka does not anticipate claim 11. M.P.E.P. §2131.

Claims 2-5 and 10 each recite combinations of features of independent claim 1, and thus claims 2-5 and 10 are not anticipated by Misaka for at least the reasons that claim 1 is not anticipated by Misaka.

Claim 14 recites the combinations of features of independent claim 11, and thus claim 14 is not anticipated by Misaka for at least the reasons that claim 11 is not anticipated by Misaka.

Applicants further assert that Misaka does not disclose "producing a layout complying with the design rules created at step (d)" as recited in claim 2. The Examiner cites column 13, lines 1-6 of Misaka as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 4. Applicants respectfully traverse and assert that Misaka instead discloses that subsequently, in step SB3, it is determined whether or not each of the circuit patterns formed in step SB2 meets the design rules. Column 13, lines 1-3. Misaka further discloses that if the answer is no, the method proceeds to Step SB 4 of modifying part of the circuit pattern not meeting the design the design rules, and then steps SB2 and SB3 are repeatedly performed. Column 13, lines 3-6. Hence, Misaka appears to disclose of modifying the circuit pattern until the circuit pattern meets the design rules. However, there is no language in the cited passage that discloses that the circuit pattern is modified to meet the design rules created at step (d) (referring to the design rule(s) to disallow at least one portion of the layout which demonstrated poor manufacturability). Thus, Misaka does not disclose all of the limitations of claim 2, and thus Misaka does not anticipate claim 2. M.P.E.P. §2131.

Applicants further assert that Misaka does not disclose "simulating how structures within the layout produced at step (e) will pattern on a wafer" as recited in claim 2. The Examiner cites column 13, lines 7-21 of Misaka as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 4. Applicants respectfully traverse and assert that Misaka instead discloses that in step SB5, specifications of OPC patterns to be made are set with respect to the circuit patterns. Column 13, lines 7-8. Misaka further discloses that the OPC pattern specifications may be set by any known technique, i.e., no matter whether the technique is rules-

based or models-based. Column 13, lines 8-11. There is no language in the cited passage that discloses simulating how structures within the layout produced at step (e) will pattern on a wafer. Thus, Misaka does not disclose all of the limitations of claim 2, and thus Misaka does not anticipate claim 2. M.P.E.P. §2131.

Applicants further assert that Misaka does not disclose "repeating steps (c) – (f) until no portions of the simulated layout demonstrate poor manufacturability" as recited in claim 3. The Examiner cites column 16, lines 21-22, 28-29 of Misaka as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 4. Applicants respectfully traverse and assert that Misaka instead discloses that steps SB1 on are performed all over again. Column 16, lines 22. Misaka further discloses that then, respective steps from step SB1 on are performed all over again. Column 16, lines 28-29. However, there is no language in the cited passage that discloses repeating steps (c) – (f). Neither is there any language in the cited passage that discloses repeating steps (c) – (f) until no portions of the simulated layout demonstrate poor manufacturability. Thus, Misaka does not disclose all of the limitations of claim 3, and thus Misaka does not anticipate claim 3. M.P.E.P. §2131.

Applicants further assert that Misaka does not disclose "modifying at least one design rule of the predetermined set of design rules to disallow a portion of the layout identified in step (c)" as recited in claim 4. The Examiner cites column 15, lines 30-33 and column 16, lines 20-21 and 27-29 of Misaka as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 4. Applicants respectfully traverse and assert that Misaka instead discloses that if the answer to the query in step SB11 is yes, then the method proceeds to step SB12, in which the design rules are modified to eliminate the pattern placement that makes the OPC ineffective. Column 15, lines 28-32. Misaka further discloses that steps SB1 on are performed all over again. Column 16, lines 22. Misaka further discloses that then, respective steps from step SB1 on are performed all over again. Column 16, lines 28-29. Hence, Misaka discloses modifying design rules to eliminate the pattern placement that makes the OPC ineffective if the OPC pattern placement rules are met as indicated in Figure 2 of Misaka. There is no language in the cited passages that discloses modifying at least one design rule of the predetermined set of design rules to disallow a portion of

the layout identified in step (c). Thus, Misaka does not disclose all of the limitations of claim 4, and thus Misaka does not anticipate claim 4. M.P.E.P. §2131.

Applicants further assert that Misaka does not disclose "wherein the initial layout is embodied in a layout data file" as recited in claim 10. The Examiner cites column 12, lines 66-67 of Misaka as disclosing the above-cited claim limitation. Office Action (6/5/2006), page 4. Applicants respectfully traverse and assert that Misaka instead discloses that next, in step SB2, circuit patterns are formed in accordance with the design rules defined. Column 12, lines 66-67. There is no language in the cited passage that discloses an initial layout is embodied in a layout data file. Thus, Misaka does not disclose all of the limitations of claim 10, and thus Misaka does not anticipate claim 10. M.P.E.P. §2131.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within Misaka, and thus claims 1-5, 10-11 and 14 are not anticipated by Misaka. M.P.E.P. §2131.

V. ALLOWABLE SUBJECT MATTER:

Applicants appreciate the allowance of claims 20-22 and the indication of allowability of claims 6-8, 12-13 and 15-19.

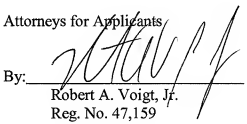
VI. CONCLUSION:

As a result of the foregoing, it is asserted by Applicants that claims 1-22 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

Attorneys for Applicants

By: 

Robert A. Voigt, Jr.
Reg. No. 47,159
Kelly K. Kordzik
Reg. No. 36,571

P.O. Box 50784
Dallas, Texas 75201
(512)370-2832

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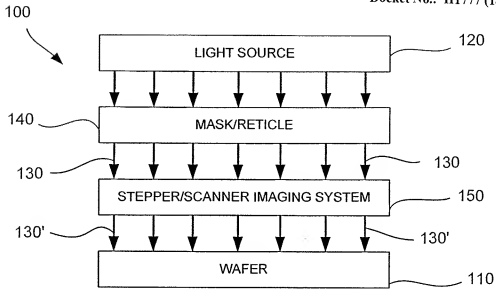


FIG. 1
(Prior Art)

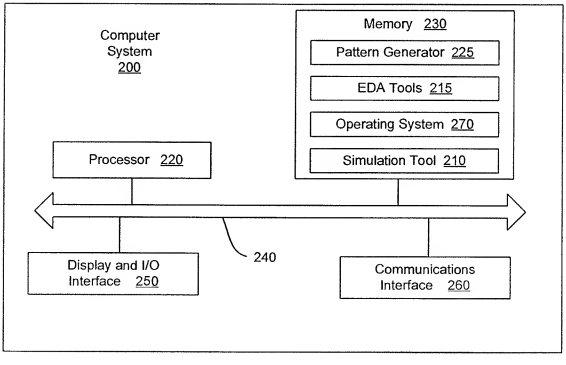


FIG. 2